#2

FORM PTO-1449 (MODIFIED)

LIST OF PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT

Applicant(s): Alexander Goldovsky
Case: 9
Serial No.: TBA
Filing Date: December 8, 2000
Group: ~~TBA~~ 2124

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NO.	DATE	NAME	CLASS/SUBCLASS	FILING DATE IF APPROPRIATE
CD	5,581,497	12/03/96	Kumar		
CD	5,337,269	08/09/94	McMahan et al.		

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NO.	DATE	COUNTRY	CLASS/SUBCLASS	TRANSLATION YES	TRANSLATION NO

OTHER DOCUMENTS

EXAMINER INITIAL	REF NO.	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
CD	1	A. Weinberger and J.L. Smith, "A One-Microsecond Adder Using One-Megacycle Circuitry," IRE Trans. on Electronic Computers, pp. 65-73, June 1956.
CD	2	T.-F. Ngai et al., "Regular, Area-Time Efficient Carry-Lookahead Adders," Journal of Parallel and Distributed Computing, Vol. 3, pp. 92-105, 1986.
CD	3	P.M. Kogge and H.S. Stone, "A Parallel Algorithm for the Efficient Solution of a General Class of Recurrence Equations," IEEE Trans. on Computers, Vol. C-22, No. 8, pp. 786-793, August 1973.
CD	4	R.P. Brent and H.T. Kung, "A Regular Layout for Parallel Adders," IEEE Trans. on Computers, Vol. C-31, No. 3, pp. 260-264, March 1982.
CD	5	D. Dozza et al., "A 3.5 NS, 64 Bit, Carry-Lookahead Adder," in Proc. Intl. Symp. Circuits and Systems, pp. 297-300, 1996.
CD	6	J. Silberman et al., "A 1.0 GHz Single-Issue 64b PowerPC Integer Processor," IEEE Intl. Solid-State Circuits Conf., pp. 230-231, February 1998.
CD	7	W. Liu et al., "A 250-MHz Wave Pipelined Adder in 2-μm CMOS," IEEE Journal of Solid-State Circuits, Vol. 29, No.9, pp. 1117-1128, September 1994.
CD	8	A. Beaumont-Smith et al., "A GaAs 32-bit Adder," IEEE Symposium Computer Arithmetic, pp. 10-17, July 1997.
CD	9	Z. Wang et al., "Fast Adders Using Enhanced Multiple-Output Domino Logic," IEEE Journal of Solid-State Circuits, Vol. 32, No.2, pp. 206-214, February 1997.

Examiner

Date Considered

9/30/03

Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

FORM PTO-1449 (MODIFIED)

LIST OF PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT

Applicant(s): Alexander Goldovsky
Case: 9
Serial No.: TBA
Filing Date: December 8, 2000
Group: ~~TBA~~ 2124

OTHER DOCUMENTS-(Cont'd)

EXAMINER INITIAL	REF NO.	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
CD		10. G. Bewick et al., "Approaching a Nanosecond: A 32 Bit Adder," IEEE International Conference on Computer Design: VLSI in Computers & Processors, pp. 221-226, October 1988.
CD		11. A. Weinberger, "High-Speed Binary Adder," IBM Technical Disclosure Bulletin, Vol. 24, No.8, pp. 4393-4398, January 1982.
CD		12. S. Knowles, "A Family of Adders," IEEE Symposium Computer Arithmetic, pp. 30-34, 1999.
CD		13. A. Goldovsky et al., "A 1.0-nsec 32-bit Prefix Tree Adder in 0.25-μm Static CMOS," 43rd Midwest Symposium on Circuits and Systems, 5 pages, August 1999.

Examiner _____ Date Considered 9/30/03

Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.